

FIG. 1 (PRIOR ART)

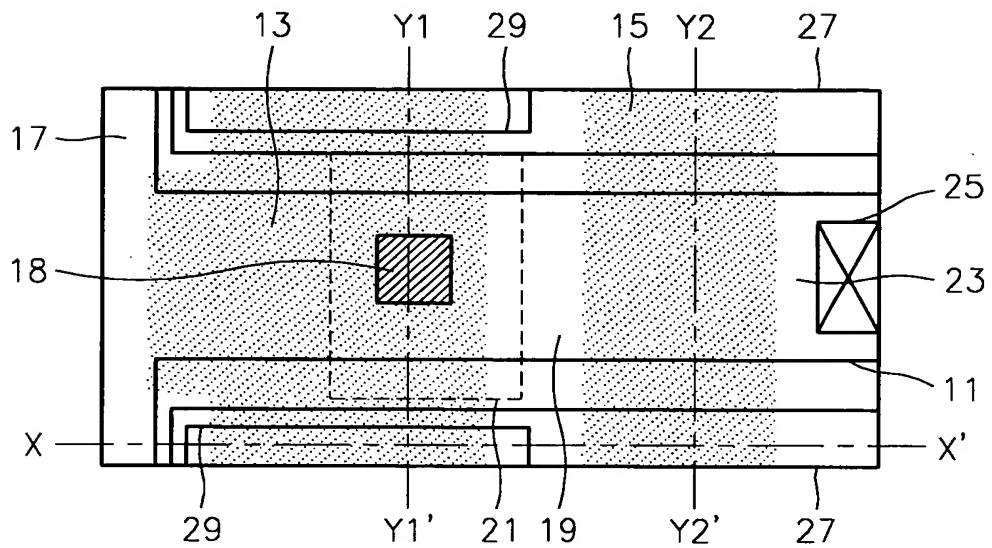


FIG. 2A (PRIOR ART)

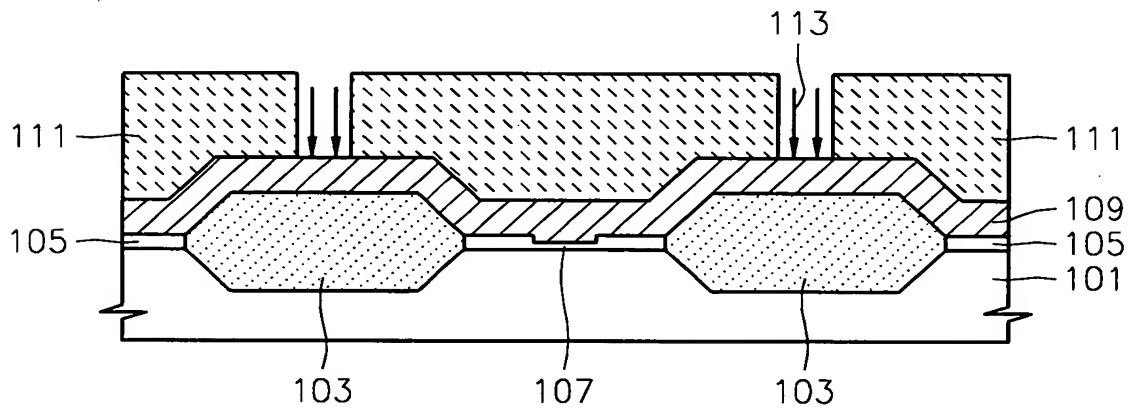


FIG. 2B (PRIOR ART)

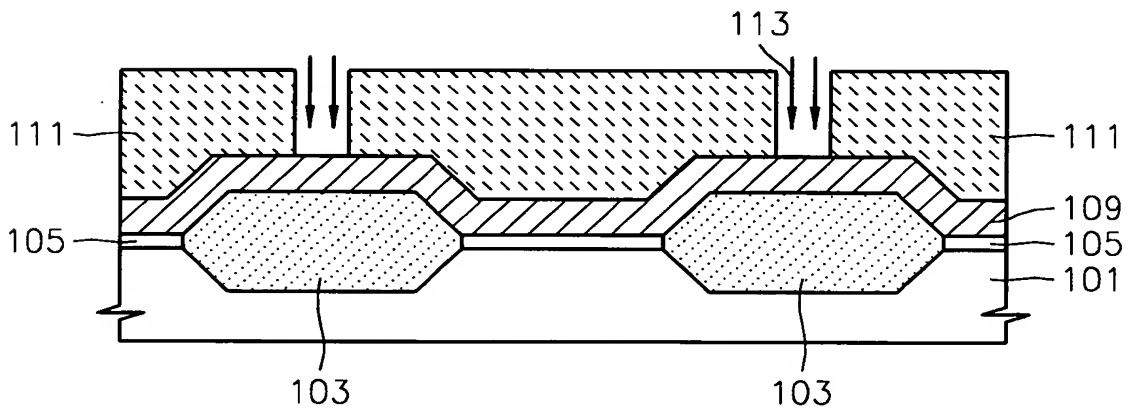


FIG. 2C (PRIOR ART)

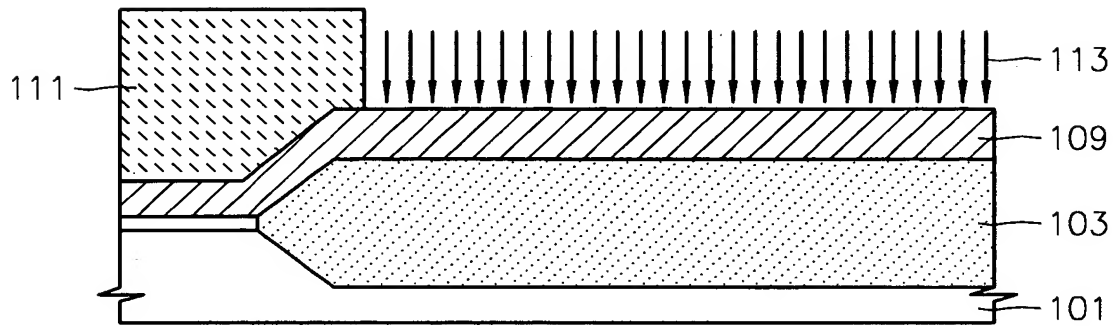


FIG. 3A (PRIOR ART)

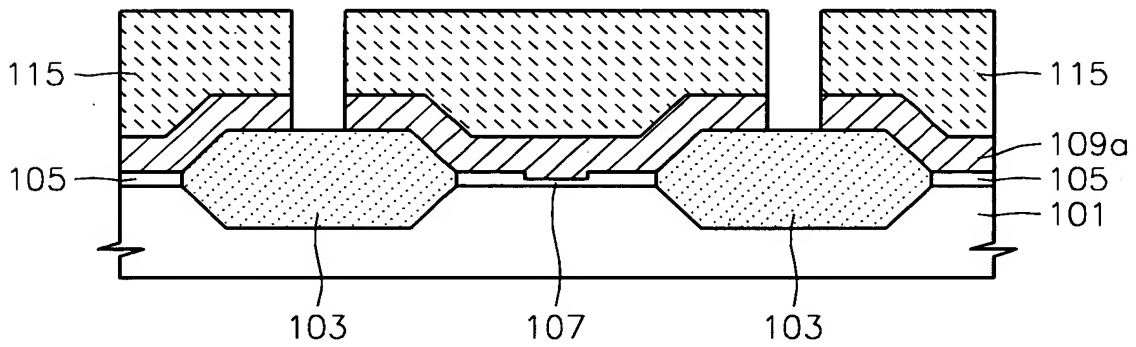


FIG. 3B (PRIOR ART)

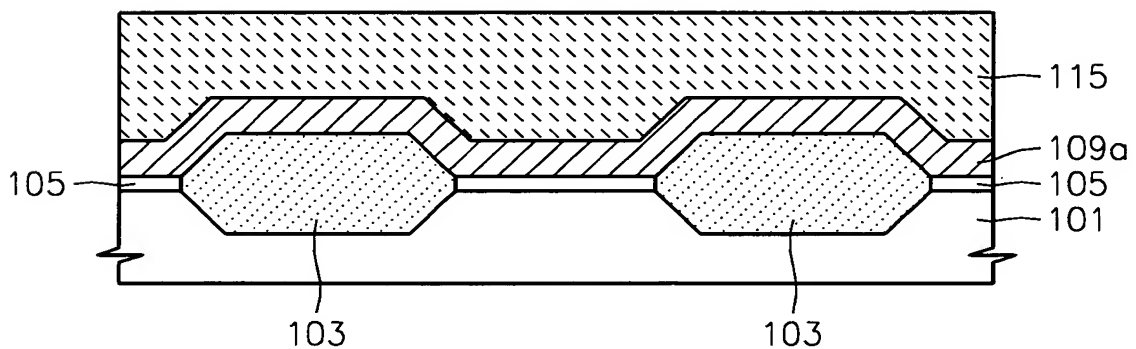


FIG. 3C (PRIOR ART)

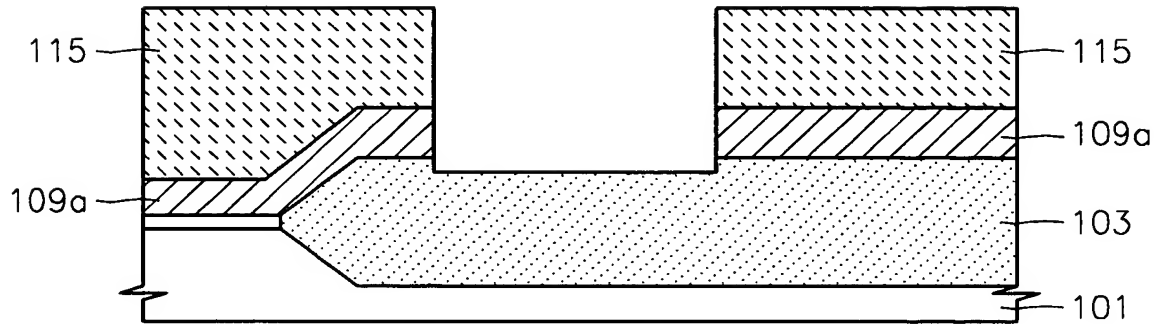


FIG. 4A (PRIOR ART)

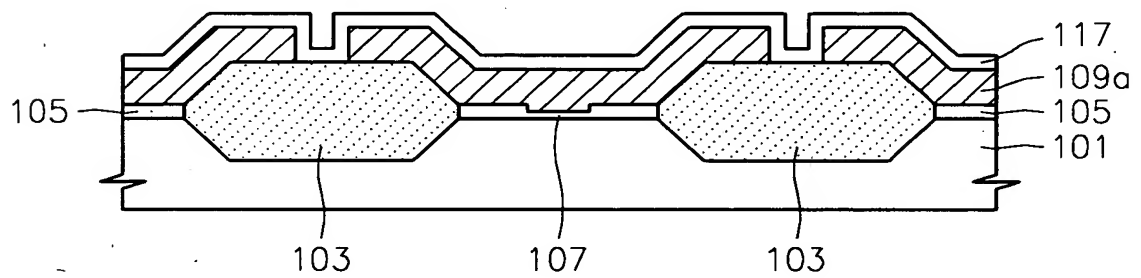


FIG. 4B (PRIOR ART)

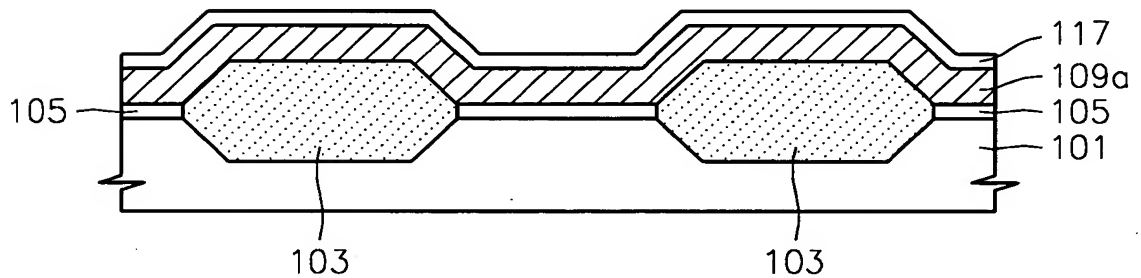


FIG. 4C (PRIOR ART)

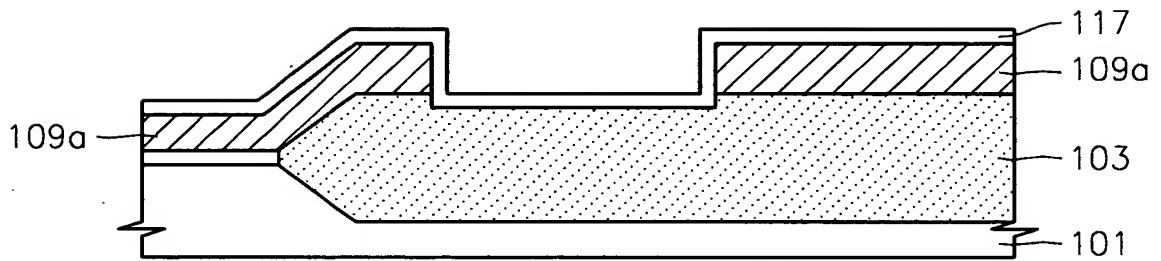


FIG. 5A (PRIOR ART)

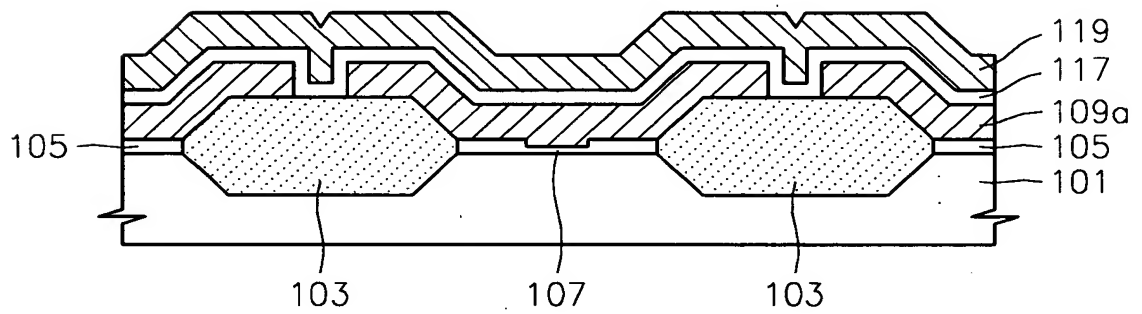


FIG. 5B (PRIOR ART)

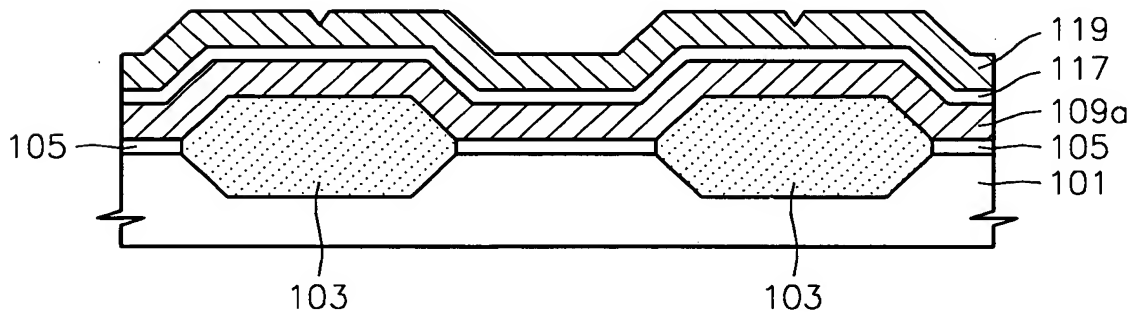


FIG. 5C (PRIOR ART)

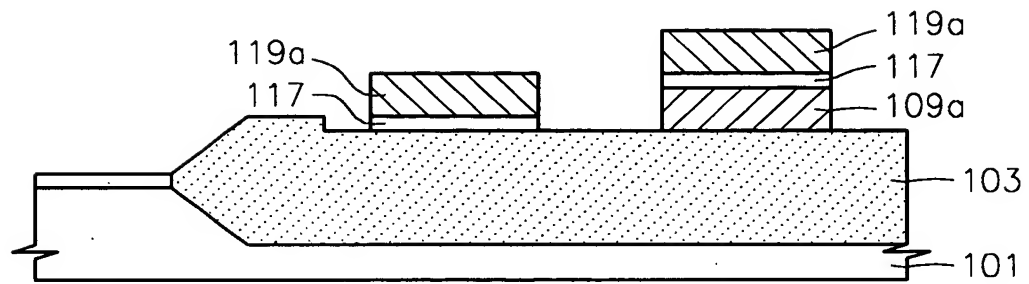


FIG. 6

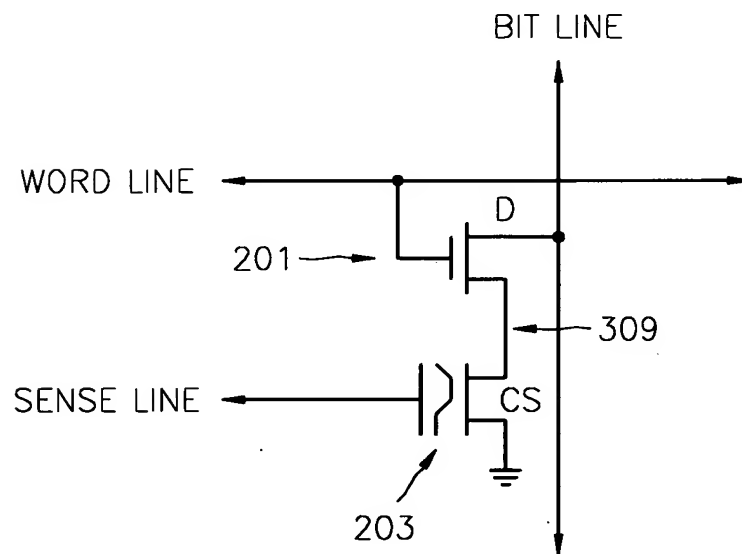


FIG. 7

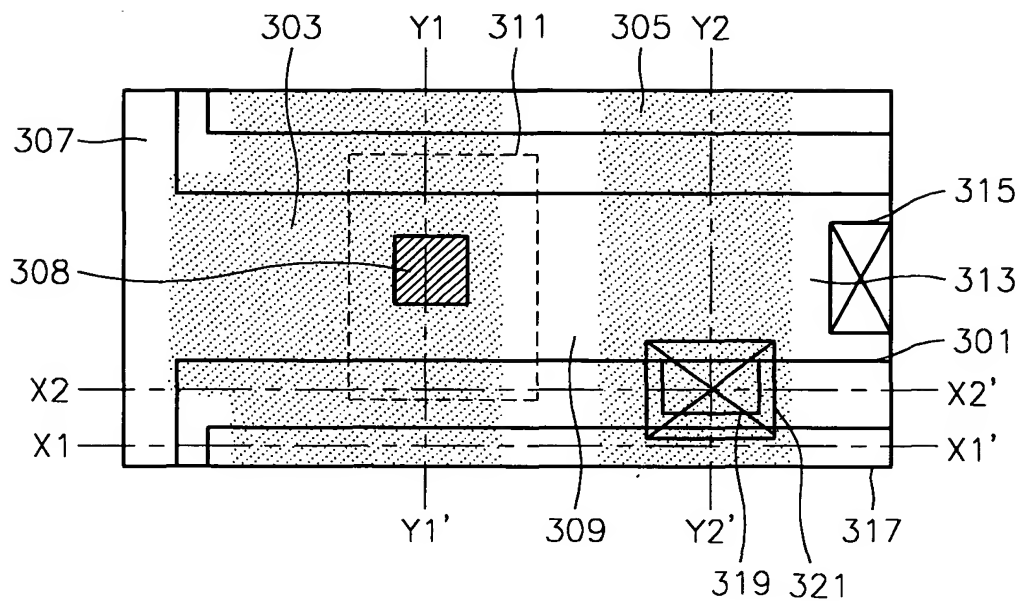


FIG. 8A

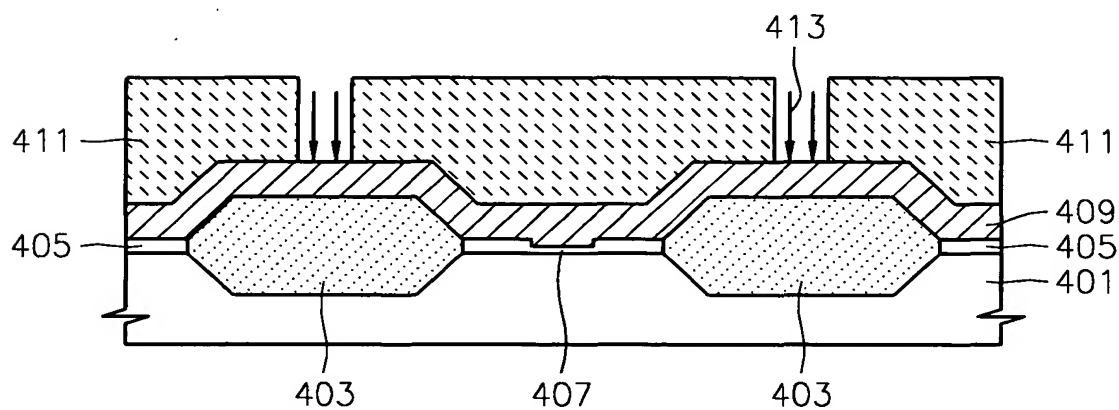


FIG. 8B

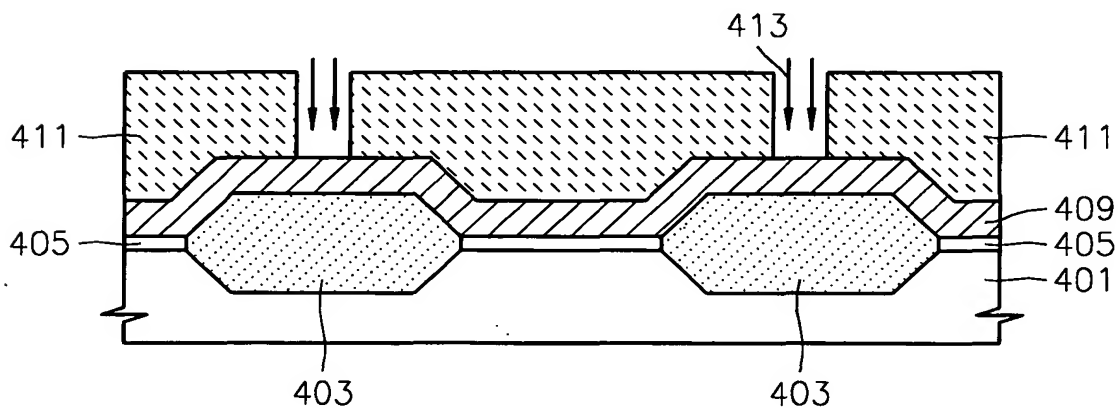


FIG. 8C

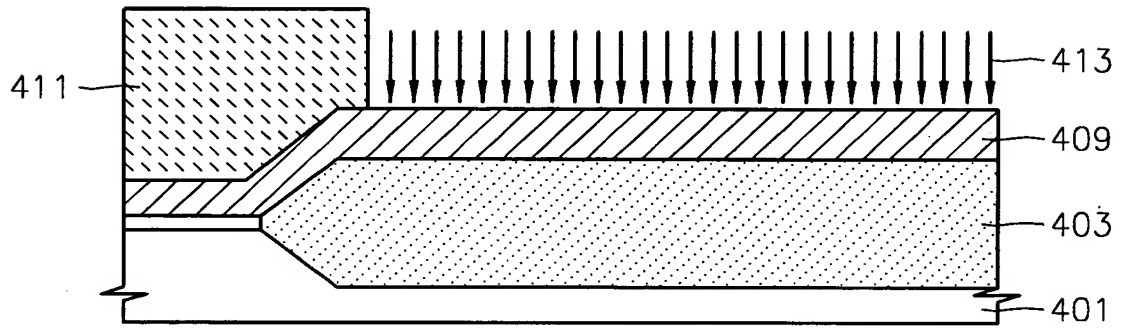


FIG. 9A

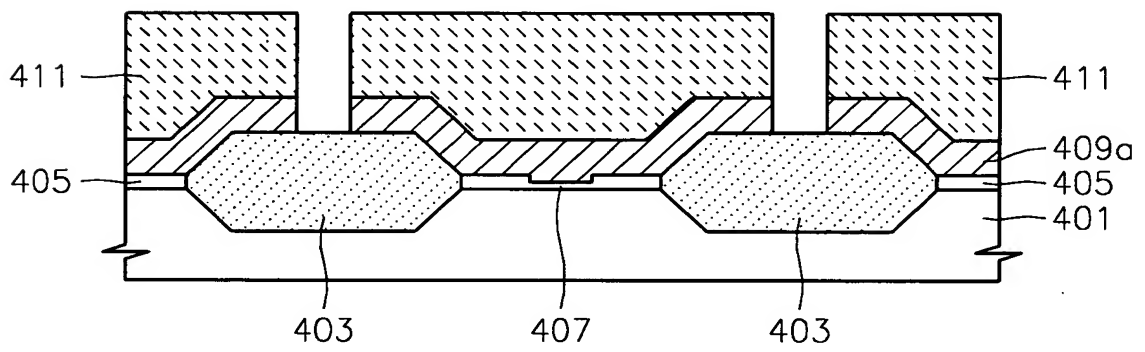


FIG. 9B

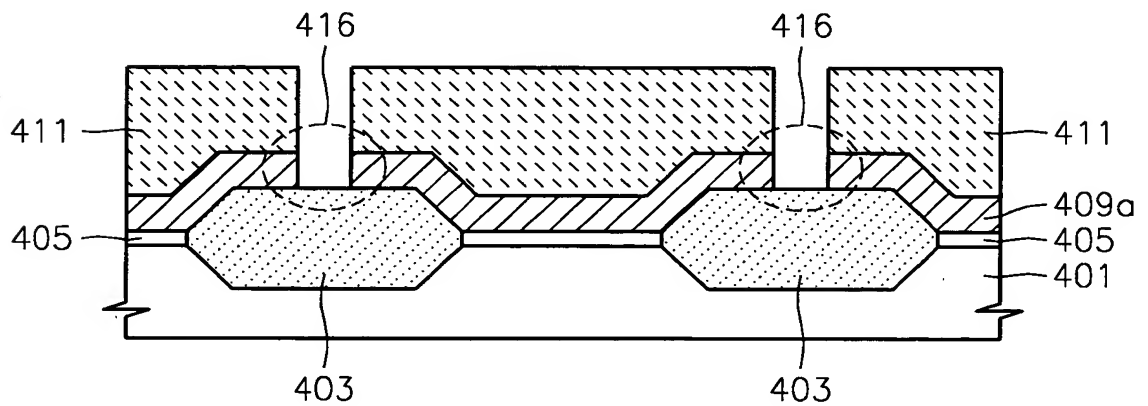


FIG. 9C

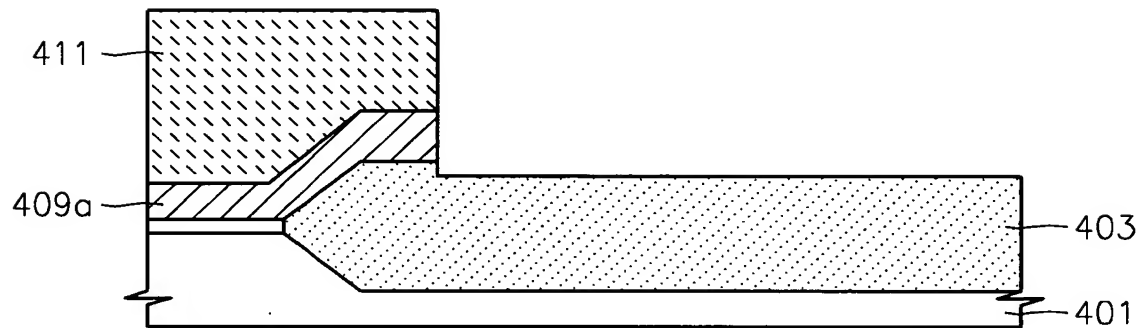


FIG. 10A

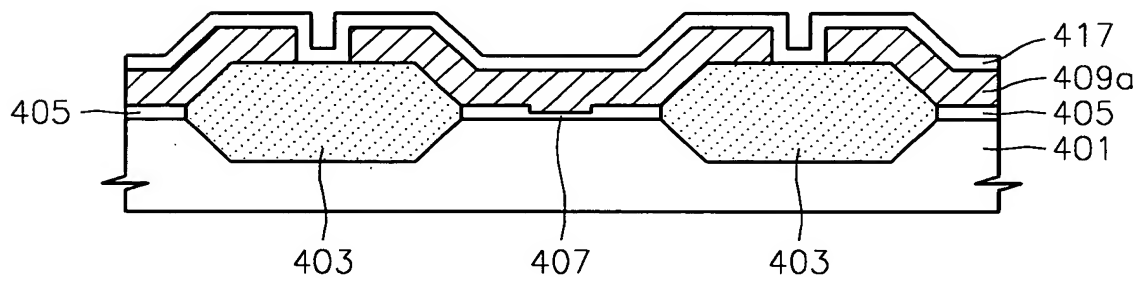


FIG. 10B

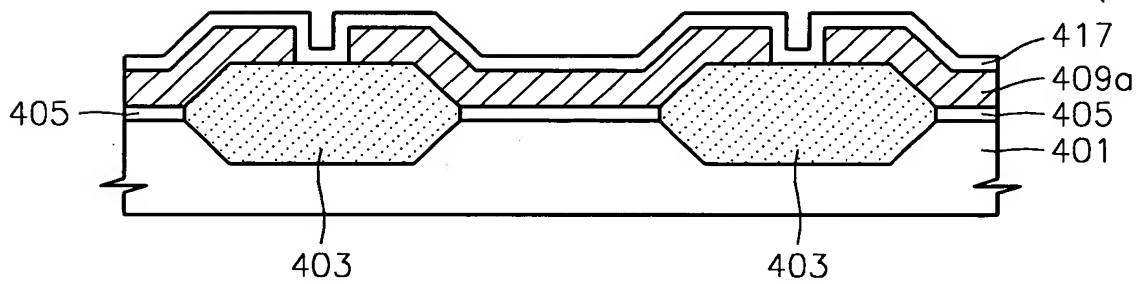


FIG. 10C

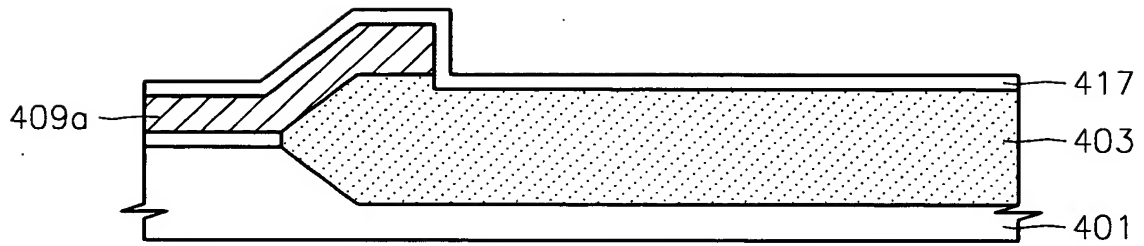


FIG. 11A

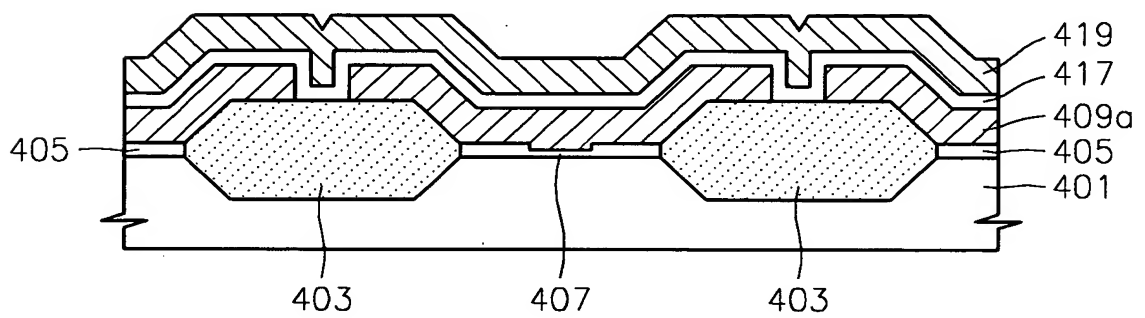


FIG. 11B

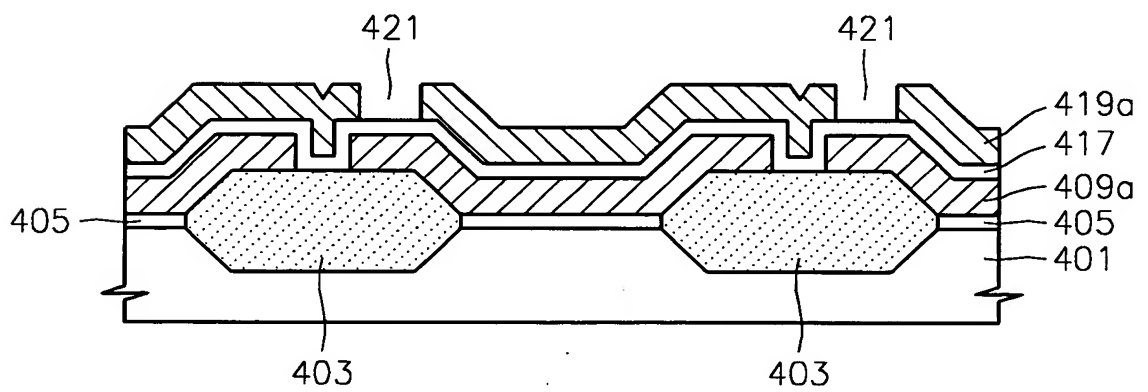


FIG. 11C

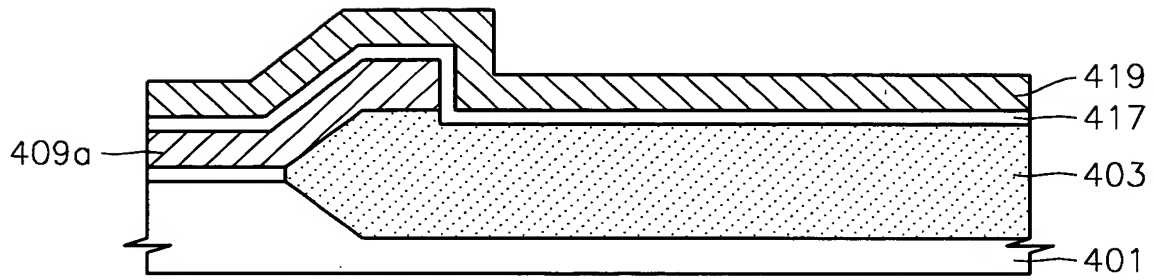


FIG. 11D

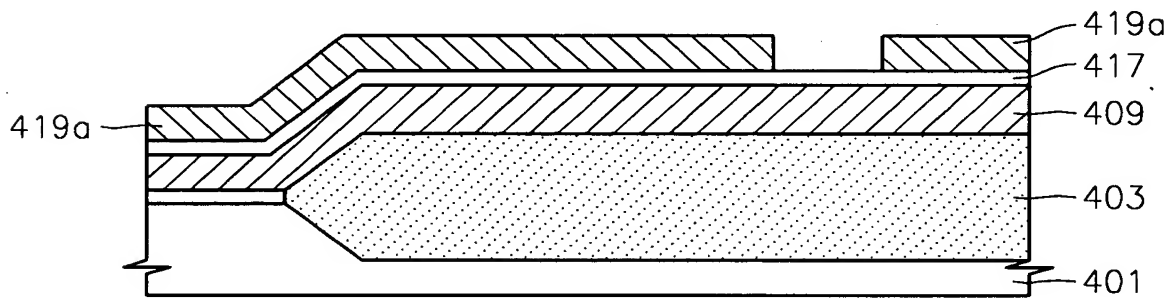
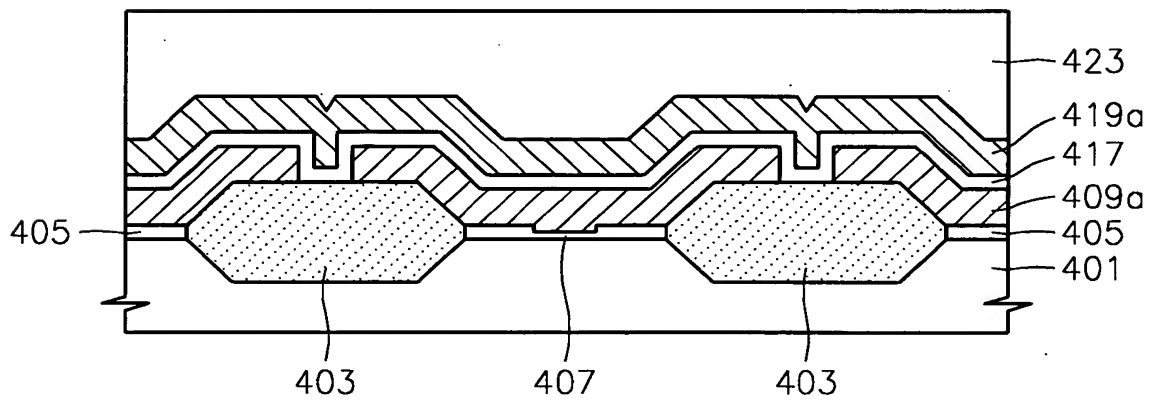


FIG. 12A



405

403

424

423

419a

417

409a

405

401

Fig. 4 is a cross-sectional view of a semiconductor device. It shows a substrate 401 with a tapered region 403. A conductive layer 405 is on the left, connected to a terminal 401. Two rectangular regions 417 are on the surface, each containing a hatched layer 419b. A top layer 423 is on the right.

FIG. 13A

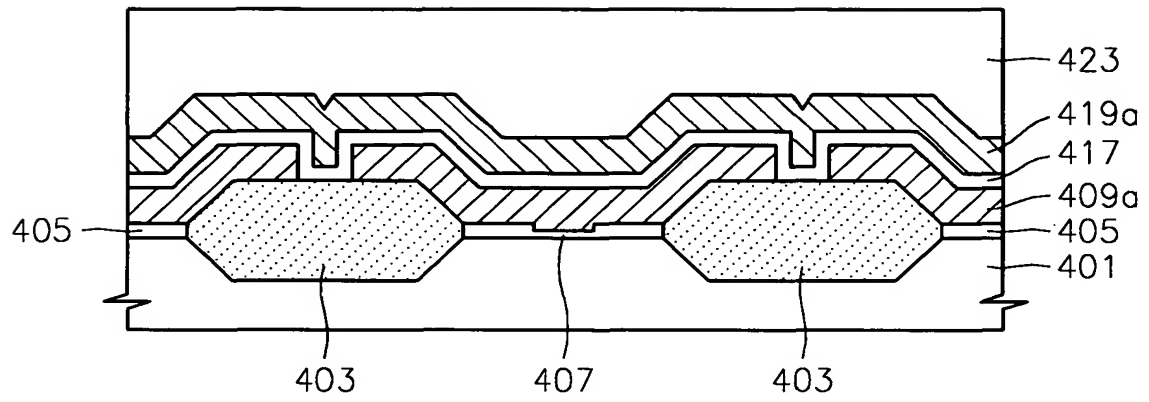


FIG. 13B

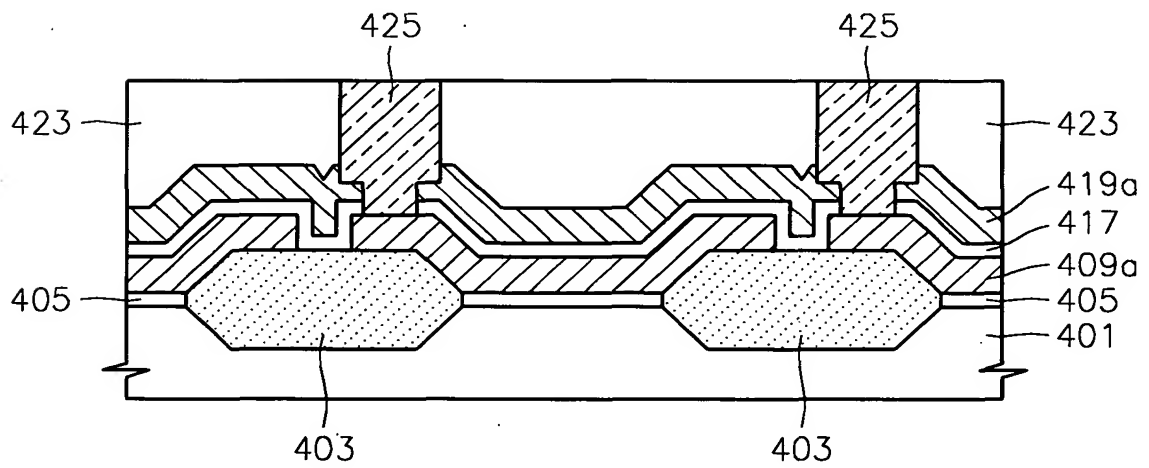


FIG. 13C

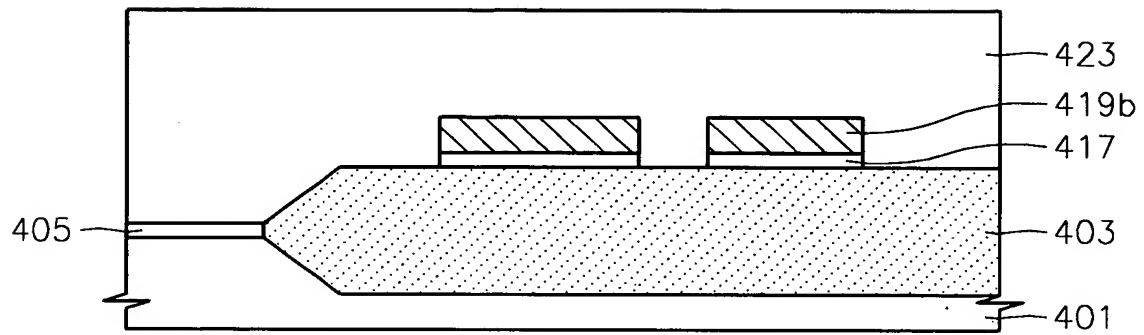


FIG. 13d

